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AMENDMENTS TO THE CLAIMS

1. (Previously Presented) A method comprising:

identifying a prefetch depth;

tracking memory subsystem requests;

selecting a time interval;

summing, for each clock cycle within the selected interval, a number of outstanding memory requests as a request sum;

dividing the request sum by a number of bus clocks within the selected interval to form an average memory subsystem occupancy level for the interval to track the average memory subsystem occupancy level as a memory subsystem response level according to the memory subsystem requests to detect the memory subsystem response level according to at least one bus transaction directed to a main memory;prefetching data according to an adjusted prefetch depth; and

adjusting the prefetch depth according to the detected memory subsystem response level.

2. (Original) The method of Claim 1, wherein the method further comprises, prior to identifying the prefetch depth:

querying a control register to determine whether prefetching is enabled; and

querying a data structure to identify a current prefetch depth as the identified prefetch depth if prefetching is enabled.

3. (Original) The method of Claim 2, wherein querying the data structure comprising:

accessing a table, including one or more entries, defining respective prefetch depths;

identifying a table entry having a valid bit enabled; and

reading a prefetched depth from the identified table entry as the identified prefetch depth.

4. (Previously Presented) The method of Claim 1, wherein prefetching comprises:

reading at least one data line from the main memory according to the identified prefetch depth.

5. (Previously Presented) The method of Claim 1, wherein adjusting the prefetch depth comprises:

identifying an update to a prefetch data structure;

identifying an entry within the prefetch data structure having a valid bit enabled;

reading a prefetch depth from the identified data structure entry as an updated prefetch depth; and

prefetching data according to the updated prefetch depth.

6. (Currently Amended) An article of manufacture including a machine readable storage medium having stored thereon instructions which may be used to program a system to perform a method, comprising:

identifying a prefetch depth;

tracking memory subsystem requests;

selecting a time interval;

summing, for each clock cycle within the selected interval, a number of outstanding memory requests as a request sum;

dividing the request sum by a number of bus clocks within the selected interval to form an average memory subsystem occupancy level for the interval to track the average memory subsystem occupancy level as a memory subsystem response level according to the memory subsystem requests to detect the memory subsystem response level according to at least one bus transaction directed to a main memory;prefetching data according to an adjusted prefetch depth; and

adjusting the prefetch depth a according to the detected memory subsystem response level.

7. (Original) The article of manufacture of Claim 6, wherein the method further comprises, prior to, identifying the prefetch depth:

querying a control register to determine whether prefetching is enabled; and

querying a data structure to identify a current prefetch depth as the identified prefetch depth if prefetching is enabled.

8. (Original) The article of manufacture of Claim 7, wherein querying the data structure comprising:

accessing a table, including one or more entries, defining respective prefetch depths;

identifying a table entry having a valid bit enabled; and

reading a prefetched depth from the identified table entry as the identified prefetch depth.

9. (Previously Presented) The article of manufacture of Claim 6, wherein prefetching comprises:

reading at least one data line from the main memory according to the identified prefetch depth.

10. (Original) The article of manufacture of Claim 6, wherein adjusting the prefetching comprises:

identifying an update to a prefetch data structure;

identifying an entry within the prefetch data structure having a valid bit enabled;

reading a prefetch depth from the identified data structure entry as an updated prefetch depth; and

prefetching data according to the updated prefetch depth.

11. (Previously Presented) A method comprising:

determining one or more prefetch depths;

selecting a prefetch depth;

calculating a memory subsystem response level to activate the selected prefetch depth;

calculating a memory subsystem response level to deactivate the selected prefetch depth;

storing the activation and deactivation levels for the selected prefetch depth within a prefetch data structure entry corresponding to an entry containing the selected prefetch depth;

repeating the selecting, calculating the subsystem occupancy deactivation level, calculating the subsystem activation level and storing the activation and deactivation level for each selected prefetch depth;

generating a validity bit entry for each respective prefetch depth entry in the prefetch data structure;

selecting a prefetch depth by enabling a validity bit of an entry within the prefetched data structure corresponding to a selected prefetch depth;

detecting a memory subsystem response level according to at least one bus transaction directed to a main memory; and

adjusting the selected prefetch depth according to the detected memory subsystem response level.

12. (Cancelled)

13. (Cancelled)

14. (Original) The method of Claim 11, wherein detecting the memory subsystem response level comprises:

tracking memory subsystem requests; and

tracking an average memory occupancy level as a memory subsystem response level according to the memory subsystem requests.

15. (Original) The method of Claim 14, wherein tracking the average memory occupancy level comprises:

selecting a time interval;

summing for each clock cycle within the selected interval, a number of outstanding memory requests as a request sum; and

dividing the request sum by a number of bus clocks within the selected interval to form the average memory subsystem occupancy level for the interval.

16. (Original) The method of Claim 11, wherein adjusting the prefetching comprises:

comparing the detected memory subsystem response level to activation and deactivation occupancy levels of one or more prefetching depths; and

selecting a new prefetching depth according to comparing of the memory of the detected memory subsystem response level.

17. (Previously Presented) The method of Claim 16, wherein selecting comprises:

comparing the detected memory subsystem occupancy level to a deactivation occupancy level of a current prefetching depth;

selecting a lower prefetching depth if the detected occupancy level is greater than the deactivation occupancy level;

otherwise, comparing the detected occupancy level against an activate occupancy level;

selecting a higher prefetch level if the detected occupancy level is less than an activate occupancy level of the current prefetch depth; and

otherwise, selecting a current prefetch depth as the new prefetch depth.

18. (Original) The method of Claim 14, wherein tracking memory subsystem requests comprises:

determining a depth of an in order queue as the number of outstanding memory subsystem requests.

19. (Original) The method of Claim 11, wherein detecting the memory subsystem response level comprises:

tracking subsystem memory requests; and

generating an average memory latency level as the memory subsystem response level according to the memory subsystem requests.

20. (Original) The method of Claim 19, wherein tracking memory subsystem requests comprises:

selecting a time interval;

summing, for each clock cycle within the selected interval, a number of outstanding memory requests as an outstanding request sum; and

summing, for each clock cycle within the selected interval, a number of received memory requests as a received request sum; and

dividing the outstanding request sum by the received request sum to form the average memory subsystem latency level for the interval.

21. (Previously Presented) An apparatus comprising:

prefetch control logic to identify a prefetch depth, to prefetch data from a main memory to store the prefetch data within a cache memory according to the identified prefetch depth, and to adjust the prefetch of data as changes in prefetch depth are detected;

memory occupancy detection logic to track memory subsystem requests, to select a time interval, to sum for each clock cycle within the selected interval, a number of outstanding memory requests as a request sum and to divide the request sum by a number of bus clocks within the selected interval to form an average memory subsystem occupancy level for the interval; and

prefetch depth logic to track the average memory subsystem occupancy level as a memory subsystem response level according to the memory subsystem requests to detect the memory subsystem response level according to at least one bus transaction directed to a main memory, and to adjust a prefetch depth according to the detected memory subsystem response level.

22. (Cancelled)

23. (Original) The apparatus of Claim 21, wherein the prefetch control logic to identify an update to a prefetch data structure, to identify an entry within the prefetch data structure having a valid bit enabled, to read a prefetch depth from the identified data structure entry as an updated prefetch depth, and to prefetch data according to the new prefetch depth.

24. (Cancelled)

25. (Previously Presented) The apparatus of Claim 21, wherein the prefetch depth logic further comprises:

memory latency detection logic to track subsystem memory requests, and generate an average memory latency level as the memory subsystem response level according to the memory subsystem requests.

26. (Previously Presented) A system comprising:

a memory controller coupled to a main memory; and

a processor coupled to the memory controller, the processor including:

at least one cache memory,

prefetch control logic to identify a prefetch depth, to prefetch data from the main memory to store the prefetch data within the cache memory according to the identified prefetch depth and to adjust the prefetch of data as changes in prefetch depth are detected,

memory occupancy detection logic to track memory subsystem requests, to select a time interval, to sum for each clock cycle within the selected interval, a number of outstanding memory requests as a request sum and to divide the request sum by a number of bus clocks within the selected interval to form an average memory subsystem occupancy level for the interval; and

prefetch depth adjustment logic to track the average memory subsystem occupancy level as a memory subsystem response level according to the memory subsystem requests, to detect, during prefetch of data, the memory subsystem response level according

to at least one bus transaction directed to the main memory, and to adjust a prefetch depth according to the detected memory subsystem response level.

27. (Original) The system of Claim 26, wherein the prefetch control logic to identify an update to a prefetch data structure, to identify an entry within the prefetch data structure having a valid bit enabled, to read a prefetch depth from the identified data structure entry as an updated prefetch depth, and to prefetch data according to the new prefetch depth.

28. (Cancelled)

29. (Original) The system of Claim 26, wherein the prefetch depth logic further comprises:

memory latency detection logic to track subsystem memory requests, and generate an average memory latency level as the memory subsystem response level according to the memory subsystem requests.

30. (Original) The system of Claim 26, further comprising:

an input/output controller coupled to the memory controller via an input/output bus.

31. (Cancelled)